RELATIVE DYNAMIC SKEW COMPENSATION OF PARALLEL DATA LINES

ABSTRACT OF THE DISCLOSURE

A system performs a two-step skew compensation procedure by first correcting for any phase error alignment between a parallel link clock and data signal edges of each data channel, thereby allowing the received data bits to be correctly sampled. Then, a second step is performed to "word-align" the bits into the original format, which is accomplished with a Skew Synchronizing Marker (SSM) byte in a data FIFO of each data channel. The SSM byte is transmitted on each data channel and terminates the skew compensation procedure. When the SSM byte is detected by logic in the data FIFO of each data channel, the data FIFO employs the SSM byte to initialize the read and write pointers to properly align the output data.